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1
2 These remarks follow the order of the paragraphs of the office action. Relevant portions of the
3 office action are shown indented and italicized.

4 **DETAILED ACTION**

5 *The present Office action is in response to application dated 15 July 2003.*
6 *Claims 1-20 are pending.*

7 **Drawings**

8 *1. The drawings are objected to because black boxes need to be labeled as to their*
9 *function:*

10 *- Figure 2, "30"*
11 *- Figures 6-8, "30", "70"*
12 *- Figure 10, "830"*

13 *Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to*
14 *the Office action to avoid abandonment of the application.*

15 In response, the applicants respectfully states that the drawings are corrected labeling the boxes
16 referenced above.

17 *2. The drawings are objected to as failing to comply with 37 CFR 1.84(p) (5) because they*
18 *do not include the following reference sign(s) mentioned in the description:*

19 *- Figure 2, "connector 170" (see Page 6, line 21)*
20 *- Figure 3, "90" (see Page 8)*
21 *- Figure 5, "PLB 390" (Page 15, line 13)*

22 In response, the applicants respectfully states that the drawings are corrected to include the
23 reference signs referenced above.

24 *3. The drawings are objected to as failing to comply with 37 CFR 1.84(p) (5) because*
25 *they include the following reference character(s) not mentioned in the description:*

26 *- Figure 2, "270"*

27 *Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to*
28 *the specification to add the reference character(s) in the description in compliance with*
29 *37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the*
30 *application. Any amended replacement drawing sheet should include all of the figures*
31 *appearing on the immediate prior version of the sheet, even if only one figure is being*
32 *amended. Each drawing sheet submitted after the filing date of an application must be*
33 *labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37*
34 *cm 1.121(d). If the changes are not accepted by the examiner, the applicant will be*

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notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3 In response, the applicants respectfully states that the drawing of Fig. 2 has the correct label of
4 270. The specification is corrected to this label of 270 rather than the incorrect label of 170 used
5 elsewhere. A complete set of drawings is provided herewith.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as 'means' and 'said,' should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

19 In response, the applicants respectfully states that an amended abstract is provided herewith.

20 The specification is further amended to correct labeling to be in accordance with the drawings.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall, conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Claims 8, 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 8, 12 recite the limitation "communicating data between the host computer system and a data communications network" in reference to claims 1 and 10, respectively. However claims 1 and 10 are silent regarding a host computer. There is insufficient antecedent basis for this limitation in the claims.

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1 In response, the applicants respectfully states that claims 8 and 16 (not 12) are amended to
2 overcome the rejections under 35 U.S.C. 112. Claim 12 is correct as originally filed.

3 ***Claim Rejections 35 USC § 103***

4 *8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all*
5 *obviousness rejections set forth in this Office action:*

6 *(a) A patent may not be obtained though the invention is not identically disclosed or*
7 *described as set forth in section 102 of this title, if the differences between the subject*
8 *matter sought to be patented and the prior art are such that the subject matter as a whole*
9 *would have been obvious at the time the invention was made to a person having ordinary*
10 *skill in the art to which said subject matter pertains. Patentability shall not be negated*
11 *by the manner in which the invention was made.*

12 *9. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ*
13 *459 (1966), that are applied for establishing a background for determining obviousness*
14 *under 35 U.S.C. 103(a) are summarized as follows:*

15 *1. Determining the scope and contents of the prior art.*
16 *2. Ascertaining the differences between the prior art and the claims at issue.*
17 *3. Resolving the level of ordinary skill in the pertinent art.*
18 *4. Considering objective evidence present in the application indicating obviousness or*
19 *non-obviousness.*

20 *10. This application currently names joint inventors. In considering patentability of the*
21 *claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the*
22 *various claims was commonly owned at the time any inventions covered therein were*
23 *made absent any evidence to the contrary. Applicant is advised of the obligation under 37*
24 *CFR 1.56 to point out the inventor and invention dates of each claim that was not*
25 *commonly owned at the time a later invention was made in order for the examiner to*
26 *consider the applicability of 35 U.S.C. 103(c), and potential 35 U.S.C. 102(e), (f) or (g)*
27 *prior art under 35 U.S.C. 103(a).*

28 *11. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yee et*

29 *al. [US 6,466,581 B1] in view of Feuerstein et al. [US 2002/0083341 A1].*

30 In response, the applicants respectfully states that the present invention on claims 1-20 are not
31 made obvious by a combination of Yee and Feuerstein et al. The present invention provides
32 methods, apparatus and systems "for controlling flow of data between a memory of a host
33 computer system and a data communications interface for communicating data between the host
34 computer system and a data communications network. In an example embodiment, an apparatus
35 includes a descriptor table for storing a plurality of descriptors for access by the host computer

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1 system and data communications interface. Descriptor logic generates the descriptors for storage
2 in the descriptor table. The descriptors include a branch descriptor comprising a link to another
3 descriptor in the table."

4 The cited reference of US 6,466,581 B1, to Yee, was filed on: August 3, 1998, and is entitled,
5 "Multistream data packet transfer apparatus and method." The Abstract of Yee reads, "A
6 multistream data packet transfer apparatus and method receives data for at least one stream of
7 multistream data from multiple fragments of memory, over a bus from a first processor. The first
8 processor stores multistream data in the fragmented memory. An interface controller, such as any
9 suitable logic and /or software, evaluates the received data to determine which received data is
10 usable data for a second processor. A data packer removes unusable data and packs the usable
11 data in fixed sized units to form a data packet for the second processor. The data packer packs
12 data received from different fragments of memory as a single packet for use by a DSP requesting
13 the information." This is not generally concerned with descriptors and certainly not with
14 anything that "generates the descriptors for storage in the descriptor table," in claims 1-20.

15 The further cited reference of: US 2002/0083341 A1, to Feuerstein, was filed December 27,
16 2000, and is entitled, "Security component for a computing device." The Abstract reads, "A
17 security component determines whether a request for a resource poses a security risk to a
18 computing device and verifies the integrity of the requested resource before the request is
19 allowed. For a request having arguments and a resource path with a filename that identifies the
20 resource, the security component determines that the request does not pose a security risk if the
21 resource path does not exceed a maximum number of characters, individual arguments do not
22 exceed a maximum number of characters, the arguments combined do not exceed a maximum
23 number of characters, and the filename has a valid extension. The security component verifies the
24 integrity of a requested resource by formulating a descriptor corresponding to the resource and
25 comparing the descriptor with a cached descriptor corresponding to the resource." This is not
26 concerned with: controlling flow of data between a memory of a host computer system and a data
27 communications interface for communicating data between the host computer system and a data

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1 communications network, descriptor table, or descriptor logic that generates the descriptors, or a
2 branch descriptor.

3 Thus, Feuerstein has little or no relation to the present invention. Also, Feuerstein has little or no
4 relation to the invention of Yee, for multistream data packet transfer. Also, there is apparently no
5 reason to combine Yee, in US Cl. 370/428, with Feuerstein, in US Cl. 713/201, except in an
6 attempt to allegedly find a combination of apparently unrelated inventions to allegedly put
7 together, and/or make obvious, the combination of elements in claims 1-20. An office action
8 may not employ hindsight in deciding obviousness of the invention in claims 1-20. It is indeed
9 not obvious to combine elements in Yee's patent directed to multistream data packet transfer,
10 with the unrelated Feuerstein patent directed to, "Security component for a computing device."
11 Furthermore, there is no reference in Feuerstein, the later patent, that it be combined with Yee.
12 It is known that an office action may not make a combination of references that is not referred to
13 in at least one of the references. Furthermore, even if the combination would produce the
14 invention in claims 1-20, (which it does not), a new combination of known parts having the
15 advantages described in the present specification is novel and patentable.

16 Regarding claim 1, Yee et al. teaches an apparatus (see Abstract) including a
17 descriptor including a descriptor table (see Figure 1, "106", "107", col. 5 lines 30-34).
18 This apparatus for controls flow of data (col. 3 lines 43-47, data stream") between first
19 and second data processing systems, col. 1 lines 15-20, "processor", "another
20 processing unit") via a memory (see "106", said descriptor table for storing a plurality
21 of descriptors for access by the first and second data processing systems; and descriptor
22 logic for generating the descriptors (see Figure 4, "200") for storage in the descriptor
23 table. However, Yee et al. Fails to teach the descriptors including a branch descriptor
24 comprising a link to another descriptor in the table. As for this limitation, Feuerstein et
25 al; teaches a descriptor having a link to another descriptor in a table (see Page 3,
26 paragraph 36 and Figure 2, "208"). At the time of the invention, one of ordinary skill in
27 the art would have been motivated to combine the cited disclosures in order to implement
28 a security function, which verifies the integrity of a requested resource, as taught by
29 Feuerstein et al. (see Abstract).

30 In response, the applicant respectfully states that exception is taken with the so called
31 equivalencies of elements in claim 1, and the cited art to Feuerstein and Yee. Claim 1 reads,

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1 1. An apparatus comprising: a descriptor table - said apparatus for controlling flow of
2 data between first and second data processing systems via a memory, said descriptor table
3 for storing a plurality of descriptors for access by the first and second data processing
4 systems; and descriptor logic for generating the descriptors for storage in the descriptor
5 table, the descriptors including a branch descriptor comprising a link to another descriptor
6 in the table.

7 A review of the cited portions of Lee fails to show or make obvious claim 1. Lee employs some
8 of the words of claim 1, but these are not used in Lee as in claim 1. Lee is not concerned with
9 "controlling flow of data between first and second data processing systems via a memory." The
10 cited portion (col. 3 lines 43-47, data stream") of Lee reads, "Storage of descriptor table
11 information for each stream is used in the memory access system, such as pointers indicating a
12 next fragmented buffer entry and size of buffer memory for a given stream." This has no
13 indication of 'control of flow'. Lee's allusion to control is not 'control of flow'. For example Lee,
14 col. 3, lines 26-28, read, "An interface controller, such as any suitable logic and/or software,
15 evaluates the received data to determine which received data is usable data for a second
16 processor." This apparently is not 'control of flow' and certainly not "controlling flow of data
17 between first and second data processing systems via a memory." Also, Lee's Fig. 2, for "a bus
18 interface control system to facilitate multistream processing," is not "controlling flow of data
19 between first and second data processing systems via a memory." Also, Lee's Fig. 5, for "a bus
20 master FIFO controller," and Lee's Fig. 6 for "a FIFO controller," are not "controlling flow of
21 data between first and second data processing systems via a memory." Also, Lee's "[A]
22 controller programs the bank of registers to allocate a single register for one stream at any given
23 time and programs bus master stream identification registers with descriptor table address
24 location and size information," is not "controlling flow of data between first and second data
25 processing systems via a memory." Thus even though similar words are used by Lee these are
26 not used to provide the element of claim 1.

27 The referenced portion of Lee, Figure 4, "200", apparently shows no allusion to using
28 descriptor logic for generating the descriptors for storage in the descriptor table." Although
29 there is reference to a descriptor table in Lee, Lee does not allude to generating descriptors as in

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1 claim 1, and not to "descriptor logic for generating the descriptors" and not to, "descriptor logic
2 for generating the descriptors for storage in the descriptor table," and certainly not to "descriptors
3 including a branch descriptor comprising a link to another descriptor in the table."

4 Furthermore, as stated in the present specification a branch descriptor comprising a link to
5 another descriptor in the table. The referenced paragraph of the cited art to Feuerstein reads,

6 "[0036] The security component 200 compares the formulated descriptor with the
7 associated cached descriptor 212 in data table 206 at block 310. If the formulated
8 descriptor and the cached descriptor are equivalent (i.e., "yes" from block 310), the
9 resource request is allowed at block 312. If the formulated descriptor and the cached
10 descriptor are not equivalent (i.e., "no" from block 310), the security component 200
11 formulates a second descriptor corresponding to the original resource 204 stored on the
12 file server 110 at block 314."

13 This apparently is a not a branch descriptor which is a link to another descriptor in the descriptor
14 table, as in claim 1. Applicant respectfully states that exception is taken with, and back up is
15 requested for, the statement above, "[A]t the time of the invention, one of ordinary skill in the art
16 would have been motivated to combine the cited disclosures in order to implement a security
17 function, which verifies the integrity of a requested resource, as taught by Feuerstein et al.
18 Thus claim 1 is not alluded to in any of the cited art separately or together. Thus claim 1 and all
19 claims that depend thereupon are allowable over the cited art.

20 *As for claim 2, Yee et al. Teaches a frame descriptor defining a data packet to be
21 communicated between a location in memory and a second processing system, identifying
22 a location in the memory (see col. 3 lines 43-49).*

23 In response, the applicant respectfully states that exception is taken with the so called
24 equivalencies of elements in claim 2, and the cited art to Yee. Claim 2 reads,

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1 2. An apparatus as claimed in claim 1, wherein the descriptors generated by the descriptor
2 logic comprise a frame descriptor defining a data packet to be communicated between a
3 location in the memory and the second data processing system, and a pointer descriptor
4 identifying the location in the memory.

5 The cited portions of Yee, col. 3 lines 43-49, reads,

6 "Storage of descriptor table information for each stream is used in the memory access
7 system, such as pointers indicating a next fragmented buffer entry and size of buffer
8 memory for a given stream."

9 A review of the cited portions of Yee shows that neither this or the rest of Yee apparently makes
10 any reference to 'a frame descriptor', 'descriptor logic', 'descriptors generated by the descriptor
11 logic', and certainly not to "descriptors generated by the descriptor logic comprise a frame
12 descriptor defining a data packet to be communicated between a location in the memory and the
13 second data processing system, and a pointer descriptor identifying the location in the memory,"
14 of claim 2. Yee's use of the words descriptor, descriptor table, stream and pointer are not
15 representative of, nor allude to, the elements formed by the particular combinations of some
16 similar words, in claim 2. Thus claim 2 is allowable over the cited art for itself and because it
17 depends on allowable claim 1.

18 *As for claims 3 and 4, Yee et al. Teaches an apparatus for data transfer involving
19 transfers of data from a processor to another processing unit (see col. 1, lines 15-20).
20 However, the combination of references does not specify the memory comprising the
21 descriptor table as part of a second or first processing system. As for this limitation, Yee
22 et al. Teaches the memory as part of Figure 1 (see "100"). Therefore, it would have been
23 obvious to include it as part of the first or second processing units since Yee et al, teaches
24 this as part of the same apparatus (See Figure 1, "102").*

25 In response, the applicant respectfully states that exception is taken with the so called
26 equivalencies of elements in claims 3 and 4, and the cited art to Yee. The statement above
27 admits that Yee does not allude to the elements of claims 3 and 4. It probably makes no
28 difference to Yee where memory is located. However, in claims 3 and 4 it makes a difference.
29 Claims 3 and 4 are used to provide claim differentiation. Thus each of claims 3 and 4 is
30 allowable over the cited art for itself and because it depends on allowable claim 1.

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1 As for claims 5, Yee et al. Fails to teach the descriptors including a branch descriptor
2 comprising a link to another descriptor in the table. As for this limitation, Feuerstein et
3 al. Teaches a plurality of descriptors linked together (see Page 3, paragraphs 36-37,
4 "cached descriptor", "formulated descriptor", "second descriptor". Figure 2, "208").
5 At the time of the invention, one of ordinary skill in the art would have been motivated to
6 combine the cited disclosures for the reasons stated above.

7 In response, the applicant respectfully states that exception is taken with the so called
8 equivalencies of elements in claim 5; and the cited art to Feuerstein and Yee. Claim 5 reads,

9 5. An apparatus as claimed in claim 1, wherein the descriptor table comprises a plurality
10 of descriptor lists sequentially linked together via branch descriptors therein.

11 Furthermore, as stated in the present specification a branch descriptor comprising a link to
12 another descriptor in the table. The above referenced paragraph 36 of the cited art to Feuerstein
13 reads,

14 "[0036] The security component 200 compares the formulated descriptor with the
15 associated cached descriptor 212 in data table 206 at block 310. If the formulated
16 descriptor and the cached descriptor are equivalent (i.e., "yes" from block 310), the
17 resource request is allowed at block 312. If the formulated descriptor and the cached
18 descriptor are not equivalent (i.e., "no" from block 310), the security component 200
19 formulates a second descriptor corresponding to the original resource 204 stored on the
20 file server 110 at block 314."

21 This apparently is a not a branch descriptor which is a link to another descriptor in the descriptor
22 table, as in claim 5. Applicant respectfully states that exception is taken with, and back up is
23 requested for, the statement above, "[A]t the time of the invention, one of ordinary skill in the art
24 would have been motivated to combine the cited disclosures in order to implement a security
25 function, which verifies the integrity of a requested resource, as taught by Feuerstein et al. Also,
26 there is no reference in Feuerstein or Yee to "sequentially" linked list, and certainly not to

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1 "descriptor lists sequentially linked together via branch descriptors." Thus claim 5 is not alluded
2 to in any of the cited art separately or together. Thus claim 5 is allowable over the cited art for
3 itself and because it depends on allowable claim 1.

4 *As for claims 6, Yee et al. Fails to teach the descriptors table as comprising a cyclic*
5 *list. As for this limitation, Feuerstein et al. teaches a plurality of descriptors linked*
6 *together (see Page 3, paragraphs 36-37, "cached descriptor", "formulated descriptor",*
7 *"second descriptor"; Figure 2, "208") These descriptors are related in a cycle (see*
8 *Figure 3). At the time of the invention, one of ordinary skill in the art would have been*
9 *motivated to combine the cited disclosures for the reasons stated above.*

10 In response, the applicant respectfully states that exception is taken with the so called
11 equivalencies of elements in claim 6, and the cited art to Feuerstein and Yee. Claim 6 reads,

12 6. An apparatus as claimed in claim 1, wherein the descriptor table comprises a cyclic
13 descriptor list.

14 A review of the cited portions of Feuerstein et al. fail to show that Feuerstein teaches "a cyclic
15 descriptor list. The cyclic descriptor list in claim 6 is apparently not related to Feuerstein's so
16 called, "a plurality of descriptors linked together in Page 3, paragraphs 36-37, "cached
17 descriptor", "formulated descriptor", "second descriptor"; Figure 2, "208"). Figure 3 fails to
18 show that "[T]hese descriptors are related in a cycle." And applicants disagree with, and request
19 back up, for the statement above, "[A]t the time of the invention, one of ordinary skill in the art
20 would have been motivated to combine the cited disclosures for the reasons stated above." Thus
21 claim 6 is not alluded to in any of the cited art separately or together. Thus claim 6 is allowable
22 over the cited art for itself and because it depends on allowable claim 1.

23 *As for claim 7, Yee et al. teaches a first date processing system comprising a host*
24 *computer system (see Figure 1, "104").*

25 In response, the applicants respectfully states that claim 7 serves the purpose of claim
26 differentiation. It is allowable over the cited art because it depends on allowable claim 1.

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1 *As for claim 8, Yee et al, teaches a communication interface for communicating data*
2 *between a host computer system and a date network (see col. 1, lines 15-38; Figure 1).*

3 In response, the applicant respectfully states that exception is taken with the so called
4 equivalencies of elements in claim 8, and the cited art to Feuerstein and Yee. Claim 8 reads,

5 8. An apparatus as claimed in claim 1, wherein the second data processing system
6 comprises a data communications interface for communicating data between the a host
7 computer system and a data communications network.

8 Yee's having 'a host computer system and a data network' does not allude to "the second data
9 processing system comprises a data communications interface for communicating data between
10 the a host computer system and a data communications network," of claim 8. Thus claim 6 is
11 allowable over the cited art for itself and because it depends on allowable claim 1.

12 *As for claim 9, the combination of Yee et al, in view of Feuerstein et al. teaches the*
13 *limitations corresponding to the apparatus as claimed in claim 1, for controlling flow of*
14 *data between the memory of the host computer system and the data communications*
15 *interface. Furthermore, Yee et al, . teaches a communication interface for communicating*
16 *data between a host computer system and a data network (see col. 1, lines 15-38; Figure*
17 *1) and therefore also teaches the data processing system having the apparatus.*

18 In response, the applicant respectfully states that as indicated for claim 1, exception is taken with
19 the so called equivalencies of elements in claim 9, and the cited art to Yee and/or Feuerstein. It
20 was shown the cited art does not make the apparatus of claim 1. Furthermore the cited art do not
21 make obvious the invention in claim 9, which reads,

22 9. (original) A data processing system comprising: a host processing system having a
23 memory; a data communications interface for communicating data between the host
24 computer system and a data communications network, and apparatus as claimed in claim
25 1, for controlling flow of data between the memory of the host computer system and the
26 data communications interface

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1 The statement above fails to show the elements of claim 9 in the cited art. Yee and/or Feuerstein
2 apparently do not have or allude to, "a data communications interface for communicating data
3 between the host computer system and a data communications network," and certainly not
4 "apparatus as claimed in claim 1, for controlling flow of data between the memory of the host
5 computer system and the data communications interface," as in claim 9. Thus claim 9 is
6 allowable over the cited art for itself and because it depends on allowable claim 1.

7 *Regarding claim 10, the combination of Yee et al, in view of Feuerstein et al, teaches the*
8 *limitations corresponding to the apparatus as claimed in claim 1, for controlling flow of*
9 *data between first and second data processing systems via a memory. Therefore, the*
10 *combination of references teaches also steps for the method directed to the apparatus.*
11 *Independent claim 10 is rejected under the same rationale.*

12 In response, the applicant respectfully states that exception is taken with the so called
13 equivalencies of elements in claim 6, and the cited art to Feuerstein and Yee. Claim 10 reads,

14 10. (original) A method comprising controlling flow of data between first and second data
15 processing systems via a memory, the step of controlling comprising: storing in a
16 descriptor table a plurality of descriptors for access by the first and second data
17 processing systems; and by descriptor logic, generating the descriptors for storage in the
18 descriptor table, the descriptors including a branch descriptor comprising a link to another
19 descriptor in the table.

20 The response to the apparatus of claim 1, is similarly appropriate to claim 10. There is no
21 showing that the cited art to Feuerstein and/or Yee allude to or make the steps of method claim
22 10 obvious, "for controlling flow of data between first and second data processing systems via a
23 memory." Thus claim 10 is allowable over the cited art.

24 *As for dependent claims 11-16, the combination of references teaches also teaches the*
25 *steps for the method directed to the apparatus, which previously rejected in claims 2-5*
26 *and 7-8 Accordingly, dependent method claims 11-16 are rejected under the same*
27 *rationale.*

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1 In response, the applicants respectfully states that the response given above overcoming the
2 rejections in claims 2-5 and 7-8, are similarly applicable to the rejection of dependent method
3 claims 11-16. Thus it was shown that the elements in claims 11-16 are not alluded to in any of
4 the cited art separately or together. Thus each of claims 11-16 is allowable over the cited art for
5 itself and because it depends on allowable claim 10.

6 *As for claims 17-18, the combination of Yee et al. In view of Feuerstein et al. teaches
7 the limitations corresponding to the apparatus as claimed in 1 and 9, for controlling flow
8 of data between the memory of the host computer system and the data communications
9 interface. Therefore, the combination also teaches the computer program product
10 comprising a computer usable medium, having computer readable program code
11 means embodied therein directed to the apparatus.*

12 In response, the applicants respectfully states that the response to the apparatus of claim 1, is
13 similarly appropriate to claims 17-18. There is no showing that the cited art to Feuerstein and/or
14 Yee allude to or make the steps of method claim 10, claims 17-18 obvious, "for controlling
15 flow of data between first and second data processing systems via a memory."

16 Furthermore, claims 17-18 are Beauregard computer type claims, which the MPEP and the courts
17 have shown have a specific use in invention protection. This is indeed not taught by the
18 combined cited art. Applicants request backup for the statement above, "the combination also
19 teaches the computer program product comprising a computer usable medium, having computer
20 readable program code means embodied therein directed to the apparatus." Thus claim 10 is
21 allowable over the cited art. Thus each of claims 17 and 18 is allowable over the cited art for
22 itself and because it depends on an allowable claim.

23 *As for claim 19, the combination of Yee et al, in view of Feuerstein et al. teaches the
24 limitations corresponding to the method as claimed in claim 10, for controlling flow of
25 data between first and second data processing systems. Therefore, the cited combination
26 also teaches the article of manufacture comprising a computer usable medium having
27 computer readable program code means embodied therein for causing the controlling of
28 the flow directed to the apparatus.*

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1 In response, the applicants respectfully states that is was shown above that the cited art does not
2 allude to or make claim 10 obvious. The cited art to Feuerstein and/or Yee do not allude to or
3 make the steps of method claim 10, claim 19 obvious, "for controlling flow of data between
4 first and second data processing systems via a memory."

5 Furthermore, claim 19 is a Beauregard computer type claims, which the MPEP and the courts
6 have shown have a specific use in invention protection. This is indeed not taught by the
7 combined cited art. Applicants request backup for the statement above, "the cited combination
8 also teaches the article of manufacture comprising a computer usable medium having computer
9 readable program code means embodied therein for causing the controlling of the flow directed
10 to the apparatus." Thus claim 10 is allowable over the cited art. Thus claim 19 is allowable over
11 the cited art for itself and because it depends on allowable claim 10.

12 *As for claim 20, the combination of Yee et al, in view of Feuerstein et al. teaches the*
13 *limitations corresponding to the method as claimed in claim 10, for controlling flow of*
14 *data between first and second data processing systems. Therefore, the cited combination*
15 *also teaches the program storage device readable by machine tangibly embodying a*
16 *program directed to the method as in claim 10.*

17 In response, the applicants respectfully states that is was shown above that the cited art does not
18 allude to or make claim 10 obvious. The cited art to Feuerstein and/or Yee do not allude to or
19 make the steps of method claim 10, claim 20 obvious, "for controlling flow of data between
20 first and second data processing systems via a memory."

21 Furthermore, claim 20 is a Beauregard computer type claims, which the MPEP and the courts
22 have shown have a specific use in invention protection. This is indeed not taught by the
23 combined cited art. Applicants request backup for the statement above, "the cited combination
24 also teaches the program storage device readable by machine tangibly embodying a program
25 directed to the method as in claim 10." Thus claim 10 is allowable over the cited art. Thus
26 claim 20 is allowable over the cited art for itself and because it depends on allowable claim 10.

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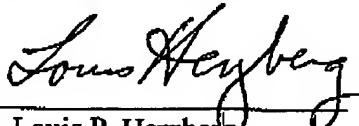
Serial No.: 10/619,960

1 It is anticipated that this response brings claims 1-20 to allowance. If any questions remain,
2 please contact the undersigned.

3 Please charge any fee necessary to enter this paper to deposit account 50-0510.

4 Respectfully submitted,

5 By:

6 
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